UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/705,895 | 11/13/2003 | Mitsuhiko Ogihara | MAE 300 | 6100 |

23995 7590 03/30/2005

RABIN & Berdo, PC
1101 14TH STREET, NW
SUITE 500
WASHINGTON, DC 20005

| EXAMINER | |
|---|---|
| PHAM, HAI CHI | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2861 | |

DATE MAILED: 03/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/705,895 | OGIHARA ET AL. | |
| | Examiner | Art Unit | |
| | Hai C. Pham | 2861 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-26 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-26 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 13 November 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 11/13/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Priority*

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### *Specification*

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means," "said" and "comprise," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

3. The abstract of the disclosure is objected to because it contains the term "comprises" at line 13, which should be avoided. Correction is required. See MPEP § 608.01(b).

### *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Norman et al. (U.S. 5,681,756) in view Asada et al. (U.S. 5,963,287).

Norman et al. discloses a method for fabricating an integrated multicolor or single color organic LED array, which comprises a substrate (12), a first thin semiconductor film (electron transport layer 14 and organic layer 15 generally very thin) (col. 3, lines 5-16) disposed on and bonded to the substrate, the first thin semiconductor film including at least one semiconductor device (each of the organic layers 15, 20, 25 corresponds to a particular color LED device), a second thin semiconductor film disposed on and bonded to the substrate, the second thin semiconductor film including an integrated circuit (integrated circuit driver using thin film transistor 50).

Norman et al. fails to teach the IC driver having a first terminal to be connected to the semiconductor device and the first individual interconnecting line formed as a thin film extending from the first thin semiconductor film over said surface of the substrate to the second thin semiconductor film, electrically connecting the semiconductor device in the first thin semiconductor film to the first terminal in the second thin semiconductor film, the second individual interconnecting line formed as a thin film electrically interconnecting the second terminal with the third terminal of the circuit pattern formed on the substrate, and the composition of the first and second interconnecting lines.

Asada et al. discloses a semiconductor device (67) having a peripheral driver circuit (driver IC 63) consisting of polycrystalline silicon thin-film transistors, a first

interconnecting line formed as a thin film (conductor layer 71a along with the anisotropic conductive film 70a) extending from the semiconductor device to the driver IC, electrically connecting the input electrode (69) of the semiconductor device to the terminal (or output electrode 64) of the driver IC, and a second interconnecting line formed as a thin film (conductor layer 71b along with anisotropic [e.g., polysilicon] conductive films 70b and 70c) connecting the second terminal of the deriver IC (input electrode 62 of driver IC 63) and the third terminal on the printed circuit board for supplying a power supply voltage and transmitting control signals (output electrode 74 of the printed circuit board 77) (Fig. 10B).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to provide the interconnecting line between the semiconductor and the driver IC in the device of Norman et al. as a thin film as taught by Asada et al. The motivation for doing so would have been to electrically interconnecting the terminals of the semiconductor to that of the driver IC in an inexpensive and effective way without the need of forming bumps as suggested by Asada et al.

Norman et al. further teaches:

- a layer of conductive material (negative contact layer 13) disposed between the first thin semiconductor film (14) and the substrate (12), the layer of conductive material being bonded formed on the substrate and the first thin semiconductor film being bonded to the layer of conductive material, whereby the first thin semiconductor film is bonded on the substrate (Fig. 1),

- the layer of conductive material (13) is a metal layer (col. 2, lines 65-66),
- the substrate has glass, resin, a ceramic, metal, or a semiconductor as its principal material (substrate 12 including a semiconductor material such as silicon) (col. 2, lines 62-64),
- the first thin semiconductor film has amorphous silicon, monocrystalline silicon, polysilicon, a compound semiconductor, or an organic semiconductor as its principal material (the semiconductor device having an organic layer 15),
- the first thin semiconductor film is an epitaxially grown compound semiconductor film (organic layer),
- the semiconductor device in said first thin semiconductor film is one of a light-emitting device, a photodetector, a Hall element, and a piezoelectric device (the layer 15 being a luminescent hole transport layer and the layer 14 an electron transport layer providing the desired light emission) (col. 3, lines 25-28), and the integrated circuit (driver IC 50) in the second thin semiconductor film includes a driver circuit for driving the semiconductor device,
- the first thin semiconductor film includes a plurality of semiconductor devices disposed at regular intervals, said semiconductor device being one of the plurality of semiconductor devices (organic layers 15, 20 and 25 forming red, green and blue organic layers disposed at regular intervals where the positive electrodes 40, 35 and 30 are respectively located) (Fig. 6),
- the first thin semiconductor film includes only one said semiconductor device (e.g., layer 15),

- a plurality of first thin semiconductor films are bonded to said surface of the substrate, said first thin semiconductor film being one of the plurality of first thin semiconductor films (Fig. 6),
- the second thin semiconductor film (driver IC 50) has recrystallized silicon, monocrystalline silicon, polycrystalline silicon, a compound semiconductor, an organic semiconductor, or a polymer as its principal material (driver IC 50 consists essentially of FETs also known as metal oxide silicon FETs made of polycrystalline silicon),
- a plurality of first thin semiconductor films are bonded to said surface of the substrate, said first thin semiconductor film being one of the plurality of first thin semiconductor films, the plurality of first thin semiconductor films being disposed in a row array, the second thin semiconductor film having a length substantially equal to a length of the linear array (the LED array being arranged at least in one row and the corresponding driver IC 66 or 70 having the same length as the LED array) (Fig. 10),
- the first and second thin semiconductor films are less than or equal to ten micrometers thick (each of the layers 14 and 15 having a thickness of 200-700 angstroms or 0.02-0.07 micrometers).

With regard to claims 7 and 18, Norman et al. in view of Asada et al. discloses all the claimed structure of the semiconductor device, and "even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its

method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (See MPEP 2113).

6. Claims 1, 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koga et al. in view of Asada et al.

Koga et al. discloses an image forming apparatus having an organic electroluminescent array exposure head (1), the apparatus includes at least a photosensitive drum (41), a developing device (44), and a transfer roller (66) (Fig. 7), wherein the exposure head comprises an array of organic EL light emitting elements (4) comprising a light emitting layer (10) and a hole injection layer (11) being bonded to the substrate (6) through the cathode layer (7), and a IC driver (5) made of thin film transistors.

However, Koga et al. fails to teach the IC driver having a first terminal to be connected to the semiconductor device and the first individual interconnecting line formed as a thin film extending from the first thin semiconductor film over said surface of the substrate to the second thin semiconductor film, electrically connecting the semiconductor device in the first thin semiconductor film to the first terminal in the second thin semiconductor film.

Asada et al. discloses a semiconductor device (67) having a peripheral driver circuit (driver IC 63) consisting of thin film transistors, a first interconnecting line formed

as a thin film (conductor layer 71a along with the anisotropic conductive film 70a) extending from the semiconductor device to the driver IC, electrically connecting the input electrode (69) of the semiconductor device to the terminal (or output electrode 64) of the driver IC (Fig. 10B).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to provide the interconnecting line between the semiconductor and the driver IC in the device of Koga et al. as a thin film as taught by Asada et al. The motivation for doing so would have been to electrically interconnecting the terminals of the semiconductor to that of the driver IC in an inexpensive and effective way without the need of forming bumps as suggested by Asada et al.

### *Pertinent Prior Art*

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Chu et al. (U.S. 6,242,358) discloses a method for fabrication thin metal film containing aluminum for forming an interconnecting line to electrically connecting semiconductor devices.

### *Contact Information*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai C. Pham whose telephone number is (571) 272-2260. The examiner can normally be reached on M-F 8:30AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (571) 272-1934. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hai Chi Pham

HAI PHAM
PRIMARY EXAMINER

March 22, 2005